LIACS - Computerarchitectuur - 2015/2016 - BSc 2de jaar

U moet deel 1 beantwoorden, dan één van de 2 andere delen. Boeken en aantekeningen zijn niet toegestaan. Iedere vraag wordt aangegeven met het aantal punten tussen haakjes. U mag vragen beantwoorden in het Engels of het Nederlands.

Tip: begin door uw tijd te verdelen tussen vragen. Bepaal dan pas de lengte van een uitleg op basis van de beschikbare tijd.

Part 1 (6pt)

a. A dual-core processor has min CPI = 22 and max IPC = 8. Explain what this means and how this is possible. [0,5pt]

b. Explain the relationship between the Memory Wall, Moore's law, Amdahl's law and Pollack's rule, and how they influenced the development of microprocessors since 1980. [2pt]

c. Explain in your own words, when possible using examples, the difference between each of the following pairs of terms [1,5pt]:

   i. throughput vs. bandwidth

   ii. D-RAM vs. S-RAM

   iii. direct mapped vs. set-associative for caches.

   iv. hardware-managed vs. software-managed for TLBs.

d. Draw a block diagram of a 4-core architecture with a GPU. Ensure your diagram includes the 4 separate cores, L1 caches, L2 cache(s), main RAM, memory interconnect, I/O interfaces and the GPU [1pt].

   On each data link in your diagram, give your own proposal for a realistic bandwidth (in bytes/second) and latency (in nanoseconds) [1pt].

   You do not need to detail the processor pipeline and memory arrays. (Note: there are many correct answers.)

Part 2 (4pt)

a. Explain the 3 possible architectures for external I/O. For each, make a simplified architecture diagram and describe the advantages and drawbacks. [1pt]

b. Explain the 3 types of hazards found in scalar processor pipelines. Provide examples for each, if possible using architecture diagrams. [1pt]

c. Explain at least 3 ways to manage data hazards in a scalar processor pipeline. For each, detail the specific advantages and drawbacks. [1pt]

d. You are tasked with choosing an architecture design for a new network switch. At the same monetary price, you are given the choice between a quad-core processor clocked at 250GHz and a single-core processor

clocked at 1GHz with a GPU attached. Which one would you choose and why? [1pt]

Part 3 (4pt)

a. Describe at least two different write policies for caches and explain when to choose one over the other. [1pt]

b. Explain why a D-RAM component needs to be refreshed over time and how this potentially impacts access times. [1pt]

c. A given D-RAM controller can answer a single load request in x second if the row for the address is already loaded in the row buffer; it needs to wait y seconds between subsequent requests, and it also needs z seconds to change rows. Express the minimum read latency, maximum read latency, and maximum read bandwidth as functions of x, y and z. [1pt]

d. You are in charge of selecting a memory configuration for a new video streaming server. You have a choice between two configurations: either 1 DRAM module at 1600MHz or 2 modules at 800MHz. Both configurations use the same DDR3 protocol (1 controller per module), are connected to the same processors, have nearly the same price. How do you choose? Why? [1pt]