

Final exam DITE: Monday, January 12, 2015 -- 14:00 to 17:00h

Task I: Design two versions (**Version A** and **Version B** below) of the combinational circuit whose input is a 4-bit number and whose output is the 2's complement of the input number:

Version A) – The circuit is a simplified two-level circuit, plus inverters as needed for the input variables.

Version B) – The circuit is made up of four identical two-input, two-output cells, one for each bit. Each cell is implemented using **only NOR gates**. The cells are connected in cascade, with lines similar to a carry between them. The value applied to the rightmost carry bit is **0**.

Important: Show and explain all the steps you do to implement the circuit above.

Task II: Implement one D flip-flop using the following components: one T flip-flop and one Multiplexer 2-to-1.

Important: Show and explain all the steps you do to implement the circuit above.

Task III: A sequential circuit with two flip-flops A and B, one input X, and one output Z is specified by the following equations:

$$A(t+1) = X(t)'A(t) + X(t)B(t)$$

$$B(t+1) = X(t)'A(t)'$$

$$Z(t) = X(t)A(t) + X(t)'B(t)'$$

Transform and implement the circuit described above as **Moore Finite State**

Machine (FSM) under the following conditions:

1. Use **only** NAND gates and SR Flip-Flops;
2. Derive and show the state table of **the Moore FSM**;
3. Derive and show the state diagram of **the Moore FSM**;
4. Draw the logic diagram of **the Moore FSM**.

Important: Show and explain all the steps you do to implement the circuit above.