

Midterm exam DITE: Wednesday, October 22, 2014 -- 10:00 to 13:00

Task I: Design a combinational logic circuit with 4 inputs that generates a 1 when the number of 0s on the inputs equals the number of 1s or the number of 0s on the inputs equals to 1. Use only 2-input NOR gates to implement the circuit.

Note: During the design you must simplify the circuit using K-map

Task II: A combinational circuit is defined by the following three Boolean functions:

$$F1 = (X+Z)' + XYZ$$

$$F2 = X'Z' + X'YZ$$

$$F3 = XY'Z + (X+Z)'$$

Design the circuit with a single 4-to-1_3-line Multiplexer and one XOR gate.

Task III: Design a 4-to-1 Multiplexer using two 2-to-1 Multiplexers with enable and four NAND gates.

Important: For all three tasks do not forget to show how you obtained the results, step by step.