Final exam DITE: Tuesday, January 8, 2013 -- 14:00 to 17:00h

Task I: Convert the following numbers from the given base to the other listed bases in the table.

Decimal	Binary	Octal	Hexadecimal
10.3125	?	?	?
?	11100101.101	?	?
?	?	623.5	?
?	?	?	A4D7.C

Important: Show and explain the conversion procedures you use and not only the final result.

Task II: A combinational circuit is defined by the following three Boolean functions:
F1 = (X+Z)' + XYZ
F2 = (X+Z)' + X'YZ
F3 = (X+Z)' + XY'Z
Implement the circuit using two 2-to-4 Decoders with enable and external NAND gates.

Task III: Simplify the Boolean function **F**(W,X,Y,Z) = ∑m(1,2,4,5,6,8,9) which has the don't-care conditions **d**(W,X,Y,Z) = ∑m(10,11,14,15) by finding all prime implicants and essential prime implicants and applying the selection rule. Note that function **F** has ***don't care*** conditions **d** that you have to take into account when simplifying function **F**. After you have simplified the function, represent it using the **logic basis NOR**. Also, draw the combinational logic circuit corresponding to the function **using only 2-input NOR gates.**
Important: Show all prime implicants and essential prime implicants as well as explain all the steps you do to simplify and represent function F.

Task IV: A sequential circuit with two flip-flops A and B, one input X, and one output Z is specified by the following equations:

A(t+1) = X(t)'A(t) + X(t)B(t)
B(t+1) = X(t)'A(t)'
Z(t) = X(t)A(t) + X(t)B(t)'

Implement the circuit described above as **Moore Finite State Machine (FSM)** under the following conditions:

1. Use **only** NAND gates and T Flip-Flops;
2. Derive and show the state table of the Moore FSM;
3. Derive and show the state diagram of the Moore FSM;
4. Draw the logic diagram of the Moore FSM.

Important: Show and explain all the steps you do to implement the circuit above.